IDEC Chip Design Contest

ΔΣ ADC based-Readout Circuit for Senputing Hardware

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Abstract

This paper proposes an energy-efficient senputing readout circuit for edge AI hardware, such as physical reservoir computing. Conventional digital-based readout circuits suffer from the limitation of power consumption due to the large data throughput required after the Analog-to-Digital Converter (ADC). To address this issue, this study designed a low-power, second-order Delta-Sigma (ΔΣ) ADC-based readout circuit using Samsung's 28nm FD-SOI process. The proposed circuit supports both a sensing mode and a computing mode, performing sensing and computation simultaneously in the analog domain by leveraging the ADC's weight adjustment capability. To improve power and area efficiency, a modulator without an input feedforward path, a level-shifting addition technique, a self-biased OTA with OTA sharing, and a counter-based decimation filter for DC inputs were adopted. In addition, an ECG-based system-level simulation was conducted to verify the feasibility of the proposed senputing architecture.

Proposed Circuit System

◆ Proposed hardware architecture

- The proposed system combines a MUX and column-parallel ΔΣ ADCs to process multi-channel analog outputs. Based on this, it supports two modes of operation.
- Sensing mode for acquisition of raw signals
- Computing mode for analog-domain computing

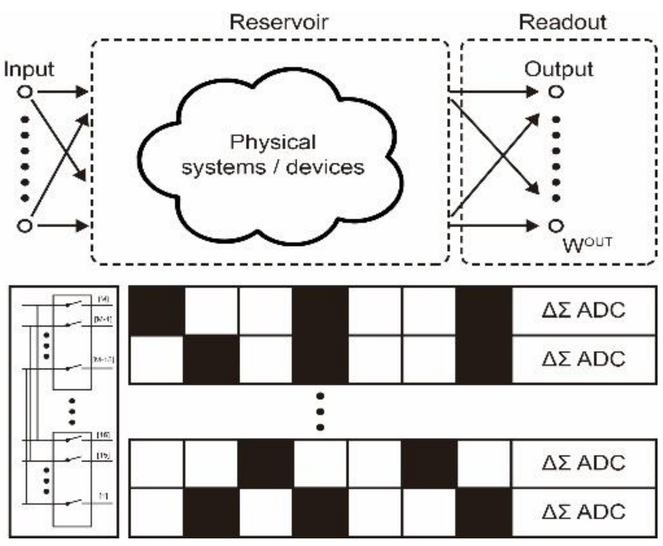

Fig. 1. Block diagram of the ΔΣ ADC-based readout circuit for RC.

◆ Modulator Implementation

- To reduce area and power, a 2nd-order ΔΣ modulator without an input feedforward path is adopted.
- A level-shifting technique is also applied to sum the outputs of the two integrators using switches and capacitors. This reduces both complexity and power consumption

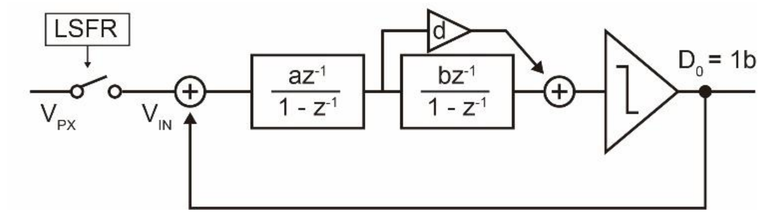

Fig. 2. CIFF architecture without input feedforward path.

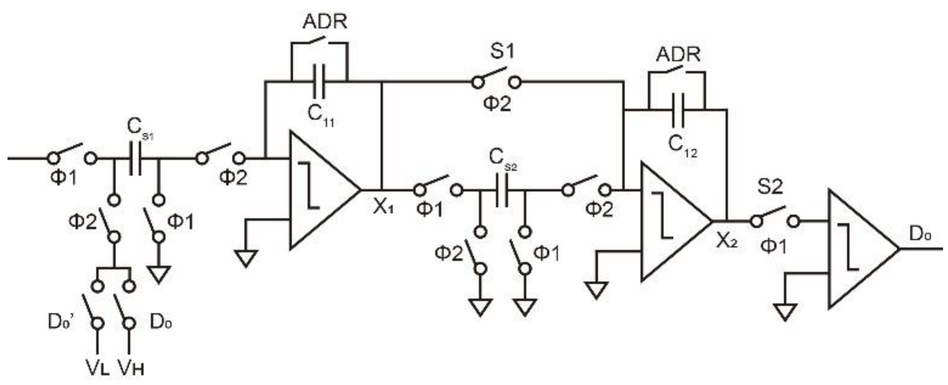

Fig. 3. Circuit diagram of the 2nd-order ΔΣ modulator.

◆ Self-bias OTA design and OTA sharing technique

- A self-biased OTA using cross-coupled inverter-based amplifiers is adopted.
- One OTA is shared between the first and second integrators in a time-division method, reducing OTA-related area and power consumption.

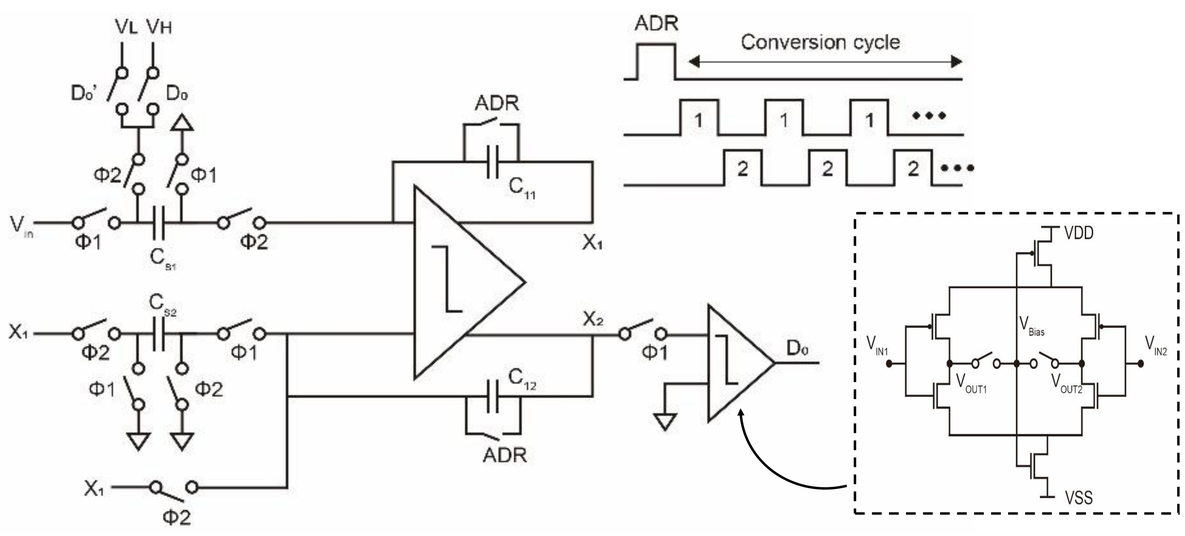

Fig. 4. OTA sharing technique for low power ΔΣ modulator.

◆ Decimation filter

- Since the target input is DC-dominant, a ripple-counter-based decimation filter is used instead of a full Sinc filter. It accumulates the number of '1's in the ΔΣ bitstream over the OSR period

◆ Simulation and measurement

- System-level simulation was performed to verify the efficiency and utility by applying Compressive Sensing (CS) with ECG signals.
- The fabricated chip is currently in the PCB design progress. The evaluation plan includes SNR, spectral analysis, power consumption, etc.

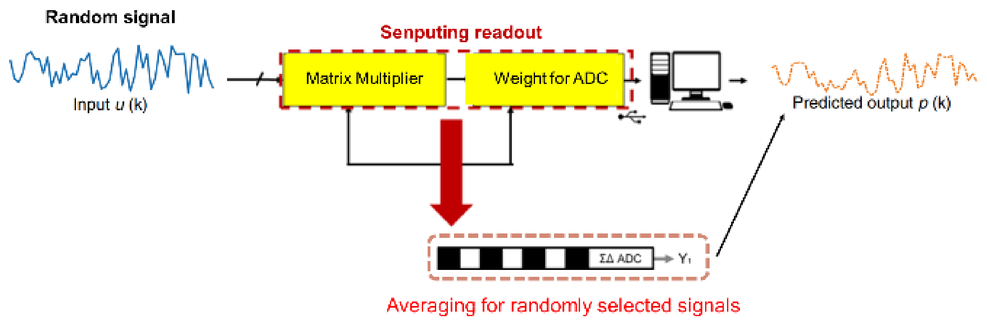

Fig. 5. System-level simulation flow of the senputing architecture.

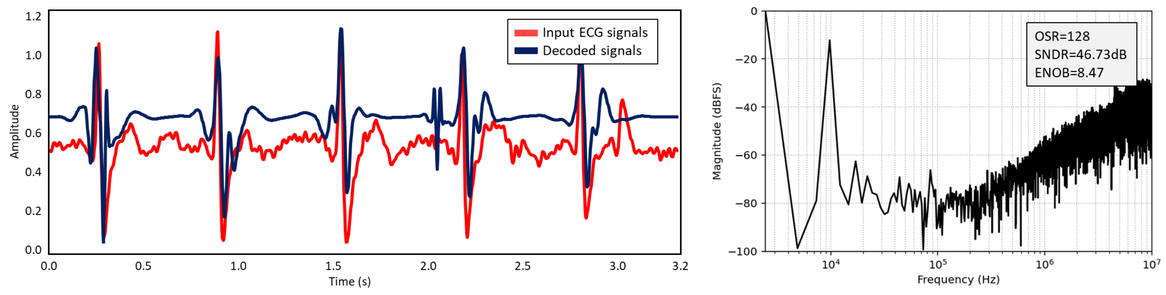

Fig. 6. System-level simulation results: decoded ECG signal (left) and output FFT spectrum (right).

Conclusion

- A low-power, high-efficiency ΔΣ ADC-based senputing readout circuit was proposed for next-generation hardware such as physical reservoir computing.
- The fabricated chip is currently in the PCB and evaluation stage, and future work will verify the energy efficiency of the proposed architecture through compressive sensing or other application-level tests.

Acknowledgement

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